



TWEPP-09 TUTORIAL



FPGA Tools and Techniques for High Performance Digital Systems

Friday, September 25, 2009 - 14:15 --> 17:45

By:

Shuvra Bhattacharyya, Professor of Computer Engineering, University of Maryland, USA
Michael Schulte, Associate Professor of Computer Engineering, University of Wisconsin, USA
Anthony Gregerson, Research Assistant in Computer Engineering, University of Wisconsin, USA

Abstract: This two-part tutorial will introduce the audience to FPGA tools and techniques that provide the ability to efficiently design, integrate, and test high performance digital systems. The first half of the tutorial will cover hardware design techniques and tools currently available from industry such as Xilinx ISE Foundation, PlanAhead Design Analysis, and ChipScope. The second half of the tutorial will cover advanced techniques and tools for complex digital system design, testing, and integration such as the Dataflow Interchange Format (DIF), the DSPCAD Integrative Command Line Environment (DICE), and Subversion (SVN) repositories.

Tutorial participants will be introduced to tools and techniques for FPGA-based design, see examples of efficient HDL coding, testing, and integration practices, gain experience with using the tools, and obtain an understanding of FPGA tool capabilities and challenges. Although the focus of the tutorial will be on FPGA-based systems, many of the tools and techniques presented can also be used to design, test, and integrate ASICs, embedded software, and other types of digital system. No previous experience with FPGA design is required.

Biographies:

Shuvra S. Bhattacharyya is a Professor in the Department of Electrical and Computer Engineering University of Maryland at College Park . He holds a joint appointment in the University of Maryland Institute for Advanced Computer Studies (UMIACS), and an affiliate appointment in the Department of Computer Science. Dr. Bhattacharyya is coauthor or coeditor of five books and the author or coauthor of more than 150 refereed technical articles. His research interests include signal processing systems, architectures, and software; embedded software; and hardware/software co-design. He received the B.S. degree from the University of Wisconsin at Madison , and the Ph.D. degree from the University of California at Berkeley . Dr. Bhattacharyya has held industrial positions as a Researcher at the Hitachi America Semiconductor Research Laboratory (San Jose, California), and Compiler Developer at Kuck & Associates (Champaign, Illinois).

Michael Schulte is an Associate Professor of Computer Engineering at the University of Wisconsin-Madison, where he directs the Madison Embedded Systems and Architectures (MESA) Lab. His research and teaching interests include FPGA-based embedded systems, domain-specific processors, and digital system design. He received a B.S. degree in Electrical Engineering from the University of Wisconsin-Madison, and M. S. and Ph.D. degrees in Electrical Engineering from the University of Texas at Austin. He has served as the Program Chair and General Chair for several internal conferences, and as an Associate Editor for the IEEE Transactions on Computers and the Journal of VLSI Signal Processing Systems.

Anthony Gregerson is a Research Assistant in Computer Engineering at the University of Wisconsin-Madison. He received his B.S. degree in Electrical Engineering from the University of Wisconsin-Platteville in 2006. His research interests include signal processing systems for high-energy physics and data-parallel computer architecture.

The tutorial presenters collaborate on an NSF-supported project called “Design and Integration of Complex Digital Systems for High Energy Physics.” This project seeks to develop novel techniques and tools to enable geographically-distributed, multidisciplinary teams of scientists and engineers to design, integrate, and test complex FPGA-based systems for upgrades to the Large Hadron Collider at CERN.

Sponsor: This tutorial is sponsored by ACEOLE, a Marie Curie Action at CERN, funded by the European Commission under the 7th Framework Programme.